ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP35

CURRENT STATUS OF THE MANUFACTURING AND TESTING OF THE BPM ELECTRONICS FOR ELETTRA 2.0

A. Gabrscek, M. Cargnelutti, U. Dragonja, Instrumentation Technologies, Solkan, Slovenia
G. Brajnik, R. De Monte, Elettra-Sincrotrone Trieste, Trieste, Italy

Abstract

In this paper we are presenting the status of the partnership between Instrumentation Technologies and Elettra Sincrotrone Trieste for the realisation of 200 BPM electronics for ELETTRA 2.0. Last year, 200 Pilot Tone Front-End (PTFE) units were successfully developed and produced. During the present year, 100 Digital Acquisition platforms, each one used to digitize and process the signals from two BPM pickups, are in production after the successful pre-series tests.

Elettra Sincrotrone Trieste was more involved in concept design, prototype development, and firmware programming, while Instrumentation Technologies was focused on design for manufacturing, implemented rigorous testing procedures, and handled the production.

During the project, it was also necessary to overcome a period of material shortages, particularly for the chips used in the digital part.

Testing during the pre-series and series production phases ensured that each unit met the desired performance criteria necessary for stabilizing long-term measurement drifts in BPM systems. Additional units were produced to account for potential failures and performance variations, ensuring that all units delivered performed to specification.

INTRODUCION

Scheduled for operation in 2026, Elettra 2.0 is set to be a next-generation of storage ring-based light sources, designed for high precision analytical studies of matter at extremely fine spatial resolutions [1]. To meet the requirements for precise beam monitoring and orbit feedback, the machine will be equipped with 168 Beam Position Monitors (BPMs) and corresponding electronics.

Within the partnership project between Instrumentation Technologies and Elettra Sincrotrone Trieste, an innovative BPM readout system [2 - 4] has been developed, produced in small series [5] and is now in the phase of large series production. The following chapter introduces the BPM electronics architecture. Later, the test procedures that were defined for Factory Acceptance Test (FAT) and Site Acceptance Test (SAT) are presented. Finally, the results of the produced instruments are described.

ELETTRA BPM ELECTRONICS

Each of the Elettra BPM electronics consist of a Data Acquisition (DAQ) platform that is used to digitize and process the BPM signals coming from two Pilot-Tone Front Ends (PTFE) that are installed in the accelerator tunnel near the BPM sensor, as described in Fig. 1.

While the PTFE consists of a single electrical board to be tested after production, the DAQ platform consists of three different boards that are tested individually before the full system is assembled – see Fig. 2. The three boards are the main digital FPGA board, one input/output (IO) board and two FPGA Mezzanine Cards (FMC) ADC boards.

A first pre-series of 7 BPM electronics systems was already tested and delivered to the customer in 2023. Among the other parameters that were measured for each produced system, special attention was dedicated to the desired performance criteria: the expected standard deviation (RMS) on the calculated beam position should be less than 100 nm with a scale factor of 10 mm and a data rate of 10 kHz.

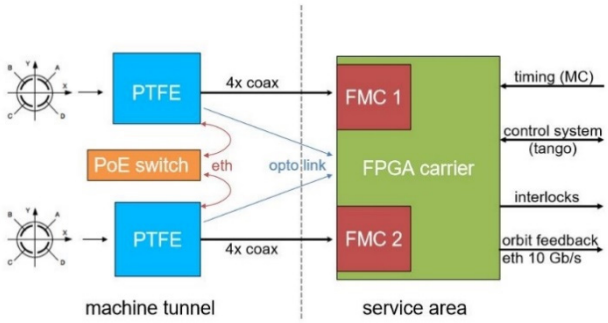

Figure 1: The Elettra 2.0 BPM electronics.

Figure 2: Assembled DAQ systems.

DEVELOPMENT OF THE TEST PROCEDURE

When a new product is developed or industrialized, before it can be mass produced, a test procedure needs to be defined. The test procedure defines the content of the tests that are performed at different stages of the production cycle: this Chapter explains how the test procedure is defined for the DAQ platform.

The first step is the execution of a system test on a limited amount of boards or devices, where their functionalities and performance is checked. The purpose is to make sure that every relevant aspect of the device can be checked or measured. After this, the manufacturing test and factory acceptance test are defined. As this project was in close

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP35

cooperation with the end user, also the site acceptance test was discussed and defined.

Manufacturing Test

The manufacturing test is an automated testing procedure executed at the production facility in order to determine whether all the produced boards are working fine, without any defects that might result from their production or due to faulty components. This procedure aims at checking every functionality of every board, and does not focus on the performance measurements that are performed at a later stage. For the purpose of the manufacturing tests execution, a special test stand is usually prepared. With it, it is possible to quickly and efficiently test any of the boards after their production. Figure 3 presents the test stand that is used for the DAQ manufacturing tests.

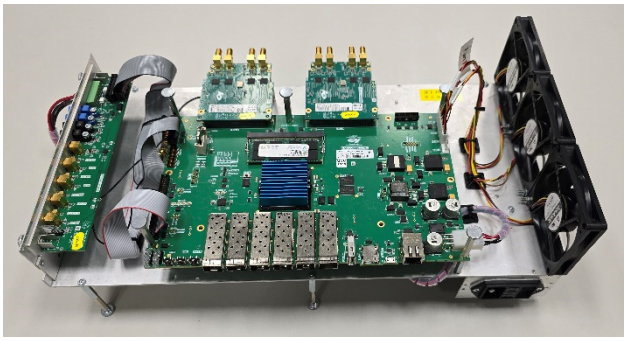

Figure 3: DAQ manufacturing test stand.

Factory Acceptance Test

After each produced DAQ system is assembled, it goes through a testing procedure called Factory Acceptance Test (FAT). This is a thorough test, performed to make sure that performance of all produced system is similar and within specifications. In order to make sure these tests are objective, it is important to have defined the pass-fail limits for each critical parameter: in this way compliance assessment can be automated. The pass-fail limits should be specified using a solid statistical base to detect real defects and eliminate as many false positives as possible.

The first part of the FAT consists of checking all the basic functionalities of a device. Visual inspection comes first, where the quality of the assembly is verified as well as the absence of physical damages. Next, the device is powered ON and all the status LEDs are checked together with the buttons, serial console and SSH connections with the internal System on Chip (SoC). Afterwards, all the sensor data is read out: board temperatures, voltages and fans speed. A simple test is also performed on the three SFP connection ports present in each device: for this, a specific IP address is assigned to each of the three ports.

The other external interfaces that are checked are all the inputs and outputs of the IO board. This is done using a couple of different loopback connections. Besides this, there is a need to check if both FMC cards manage to successfully lock to the Machine Clock (MC) frequency, to confirm the MC input is working. This signal is the reference for all the PLL loops used inside the device.

Once the device passes all the previous tests, its performance is tested. Both the two FMC cards, A and B, are tested separately, as they will be used in the real situation. Special care is necessary to avoid interference between the inputs of both cards. Figure 4 presents the test setup used for the performance tests. An RF generator with RF splitters provides a 499.654 MHz Continuous Wave (CW) signal to these cards. Among the tests performed, the ADC data is checked to confirm the expected levels. Also, the deviation between the four input channels should not exceed a specified threshold. The following is the most important part of the test: the measurement of the RMS of the calculated X and Y positions, while the RF input power is swept in a certain dynamic range.

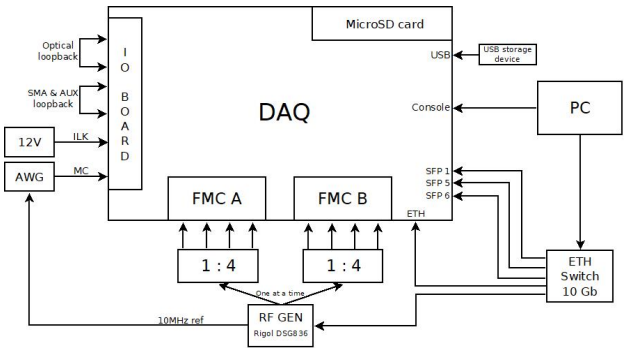

Figure 4: FAT test connection scheme.

The long-term measurement stability of these instruments is also very important: on every 10th instrument produced, a long-term test is performed by using a temperature chamber. Two PTFEs are used to compensate for thermal drift, channel variations and RF cable responses, leading to even better position RMS results.

Site Acceptance Test

Once the instruments are delivered to the customer, the Site Acceptance Test (SAT) is performed to confirm the functionality and performance of the devices. This test is conducted in a real environment, testing the device characteristics over a couple of hours or even days. The test setup is similar to the one used during FAT, where an RF generator is used to emulate the beam. The customer adds one PTFE for each tested FMC card, ensuring a whole BPM electronics system is tested.

The 10 kHz data stream is acquired through the network and averaged to obtain a 1 Hz equivalent data-rate. Channel amplitudes and positions are recorded while the pilot-tone compensation is applied.

Figures 5 and 6 below present the performance of one instrument over a 30 minute test and a 12-hour test respectively. X and Y are the non-compensated positions, Xp and Yp are the equivalent positions of the injected pilot tone, Xc and Yc are the compensated positions. One can clearly see how the compensated positions are far more stable and

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP35

have better RMS compared to uncompensated positions in both equivalent bandwidths.

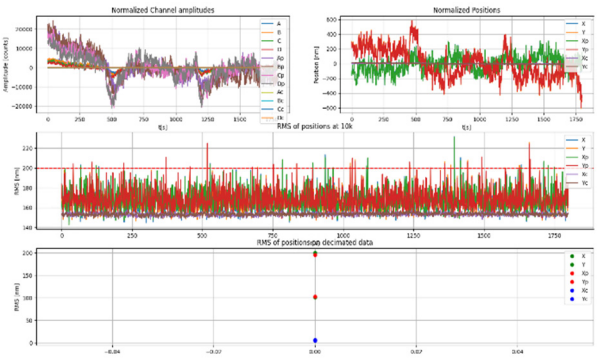

Figure 5: 30-minute-long term test results.

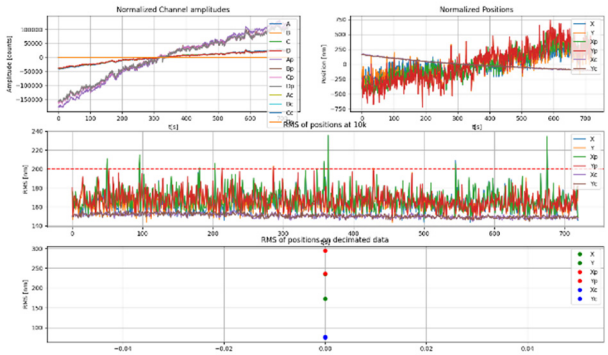

Figure 6: 12-hour long term test results.

In both figures, the upper-left graph shows the normalized channel amplitudes, the upper-right graph shows the normalized X and Y positions. The graph in the middle shows the RMS of X and Y positions acquired from the continuous 10 kHz data stream. Finally, the graph at the bottom shows RMS of X and Y positions using the decimated data.

What can be observed on the middle graph is that the non-compensated position RMS is higher than 100 nm, with a pass-fail limit set to 200 nm. This is expected since the front ends add their own noise into the signal chain: from the performed measurements, roughly 6 dB of noise is introduced.

If one looks at the RMS of the compensated position, the results are significantly improved. Indeed, the pilot-tone injection and compensation helps to remove the thermal drifts as well as the drifts along with 1/f noise. This can be seen on the bottom graphs in Figs. 5 and 6, where the compensated X and Y positions, blue dots on the graph, are in the range of 10 nm and 50 nm respectively, far below the desired 100 nm limit.

RESULTS FROM FAT TESTS ON THE PRODUCED SERIES

This chapter presents some of the key performance figures that were measured on the PTFEs and DAQ platforms during the FAT tests, for example the Signal-to-Noise ratio (SNR) for the PTFE units, while for the DAQ units, the RMS of X and Y positions will be reported.

Figure 7 shows the SNR statistics of all the tested PTFE units. The SNR was measured at the outputs of each unit, while the internal pilot-tone generator was turned on. What can be seen is the repeatability across all the tested devices: the mean value of the SNR is almost 80 dB, with a standard deviation of only 0.22 dB.

In a similar way, Figs. 8 and 9 show the comparison of the position RMS results of all the tested DAQ devices, according with the test setup presented in Fig. 4. The test was done sweeping the input RF power from 6 dBm down to -10 dBm in discrete steps. Compared to the 100 nm goal, the measured resolution is very good for the whole range: all DAQ systems are within required limits, with position RMS ranging from 50 nm to 80 nm on the applied input signal dynamic range.

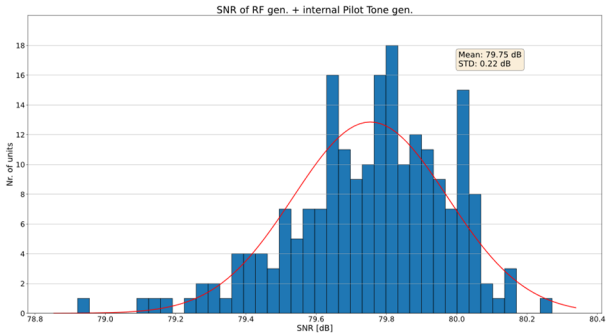

Figure 7: SNR comparison of all tested PTFEs.

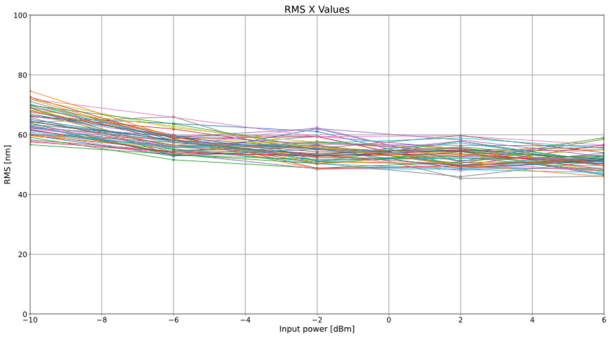

Figure 8: RMS of X positions of DAQ units.

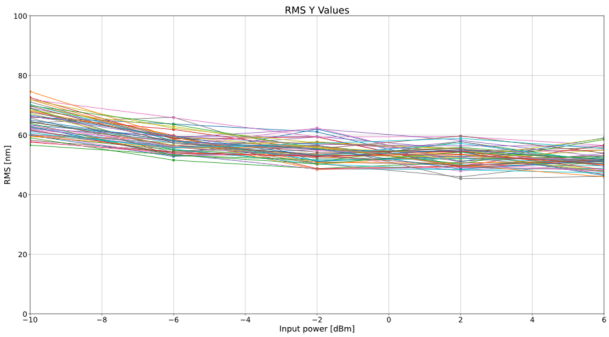

Figure 9: RMS of Y positions of DAQ units.

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP35

Table 1: Number of Boards/Units Manufactured

Board/unit	Number of boards/units
DAQ board	102
FMC board	204
IO board	102
Complete unit	102

Table 2: Statistics on Failed Boards/Units

Board/unit	Number of boards/units
DAQ board	5
FMC board	1
IO board	1
Complete unit	20

Table 3: Statistics on the Type of Identified Defects

Defect	Number
USB port	1
Buttons	2
Fans	4
RMS out of spec.	13

Among the produced devices - see Table 1, some did not pass the tests, either at the manufacturing tests stage or later during the FAT tests. Table 2 presents the statistics for all the failed boards/units that were detected. Some of the failures couldn't be detected during the manufacturing testing, since they were related to component failures, for example fans, which were not tested before all the boards being assembled in the chassis. See Table 3 for an overview on the type of defects that were identified.

Eventually, all the devices with performance out of specifications were successfully repaired. In most cases, the issue proved to be related to small metal pieces that got into the FMC connectors during the unit assembly. Once the connectors were cleaned with compressed air, all units passed the tests.

CONCLUSION

The test results of the 100 digital acquisition platforms together with 200 PTFEs confirm that the industrialization of the new BPM readout system for Elettra 2.0 was successful. All the produced devices passed the test having very similar performance.

As expected, a couple of failed units/boards were discovered. A lesson learned was to pay special attention while assembling the DAQs and to perform a last-minute cleaning before inserting FMC cards into their slots on the FPGA board. This approach will help in minimizing potential issues in future assemblies, while also saving assembly and testing time. Overall, both the PTFEs and the DAQ platforms proved to perform well together, providing at the same time, excellent beam position resolution and long term stabilization capability.

REFERENCES

[1] Elettra 2.0 webpage presentation: https://www.elettra.eu/lightsources/elettra/elettra-2-0.html

[2] G. Brajnik, S. Bassanese, S. Carrato, G. Cautero, and R. De Monte, "A Novel Electron-BPM Front End With Sub-Micron Resolution Based on Pilot-Tone Compensation: Test Results With Beam", in *Proc. IBIC'16*, Barcelona, Spain, Sep. 2016, pp. 308–311. doi:10.18429/JACoW-IBIC2016-TUPG02

[3] G. Brajnik, R. De Monte, M. Cargnelutti, P. Leban, P. Paglovec, B. Repič, "Current status of Elettra 2.0 eBPM System", in *Proc. IBIC'21*, Pohang, Rep. of Korea, September 2021, pp. 71-74. doi:10.18429/JACoW-IBIC2021-MOPP16

[4] M. Colja, S. Carrato, G. Brajnik and R. De Monte, "Design and Implementation of an FPGA-Based Digital Processor for BPM Applications", in *Proc. IBIC'22*, Krakow, Poland, September 2022, pp. 55-58. doi:10.18429/JACoW-IBIC2022-MOP14

[5] G. Brajnik, R. De Monte, M. Cargnelutti, U. Dragonja, P. Leban, P. Paglovec, "Test and Measurement Results of the Pilot Tone Front End Industrialization for Elettra 2.0", in Proc. *IBIC'22*, Krakow, Poland, September 2022, pp. 51–54. doi:10.18429/JACoW-IBIC2022-MOP13